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L13: (386) 12 and (contact)
L14: (3) 12 and (contact adj pillar)
L15: (383) (13 not 14) and (method or process)
L16: (383) 15 and (method or process)
L17: (131) 16 and (second adj (dielectric or insula
L18: (82) 17 and ((second adj (dielectric or insula
L19: (69) 18 and (capacitor with (plate or electro
L20: (66) 19 and expos$4
L21: (60) 20 and (expos$4 with (etch$4 or remov$4))
L22: (5) 21 and (ground adj (plate or electrode))
L23: (0) 20040012022.URPN.
L24: (1) "6562679".PN.
L25: (0) 6727542.URPN.
L26: (9) ("4864374" | "5229326" | "5998225" | "6236
L27: (0) 6746915.URPN.
L28: (0) 6746915.URPN.
L29: (55) 21 not 22
L30: (3) memory and capacitor and (contact adj pill
L31: (10) ("4994893" | "5045899" | "5475248" | "562
L32: (0) 6710301.URPN.

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Index	Find	<b>Browse</b>	Queue	Clear
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QB8 | USPAT, US-PGPUB, EPQ, JPQ, 18M\_TDB

R. Burała

Default operator, ☐ OR

☒ Highlight all hit terms initially

21 and (ground adj (plate or electrode))

 BRS Item
  K&R Item
  Image
  Text
  HTML

	U	I	PT	P	Document ID	Issue Dat	Pages	Title	Current OR	Current XF
1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20040012022	20040122	20	Stack-type DRAM memory structure and its manufacturing method	257/68	257/300; 257/71
2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20030132429	20030717	21	Semiconductor memory device and method for manufacturing the same	257/1	257/43; 257/E21.01
3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6746915 B2	20040608	19	Stack-type DRAM memory structure and its manufacturing method	438/253	257/296; 257/300;
4	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6727542 B2	20040427	18	Semiconductor memory device and method for manufacturing the same	257/306	257/303; 257/309
5	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 5665624 A	19970909	9	Method for fabricating trench/stacked capacitors on DRAM cells with increased capacitance	438/244	257/E27.09 47